OIPE MAY 11 2006 PATENT & TRADEMARK OFFICE

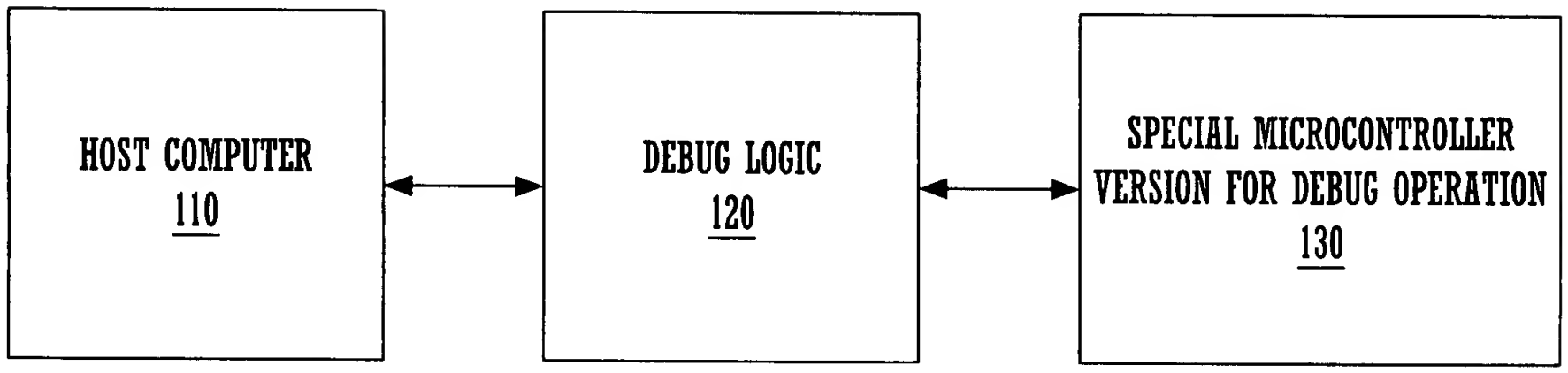

FIGURE 1
(Prior Art)

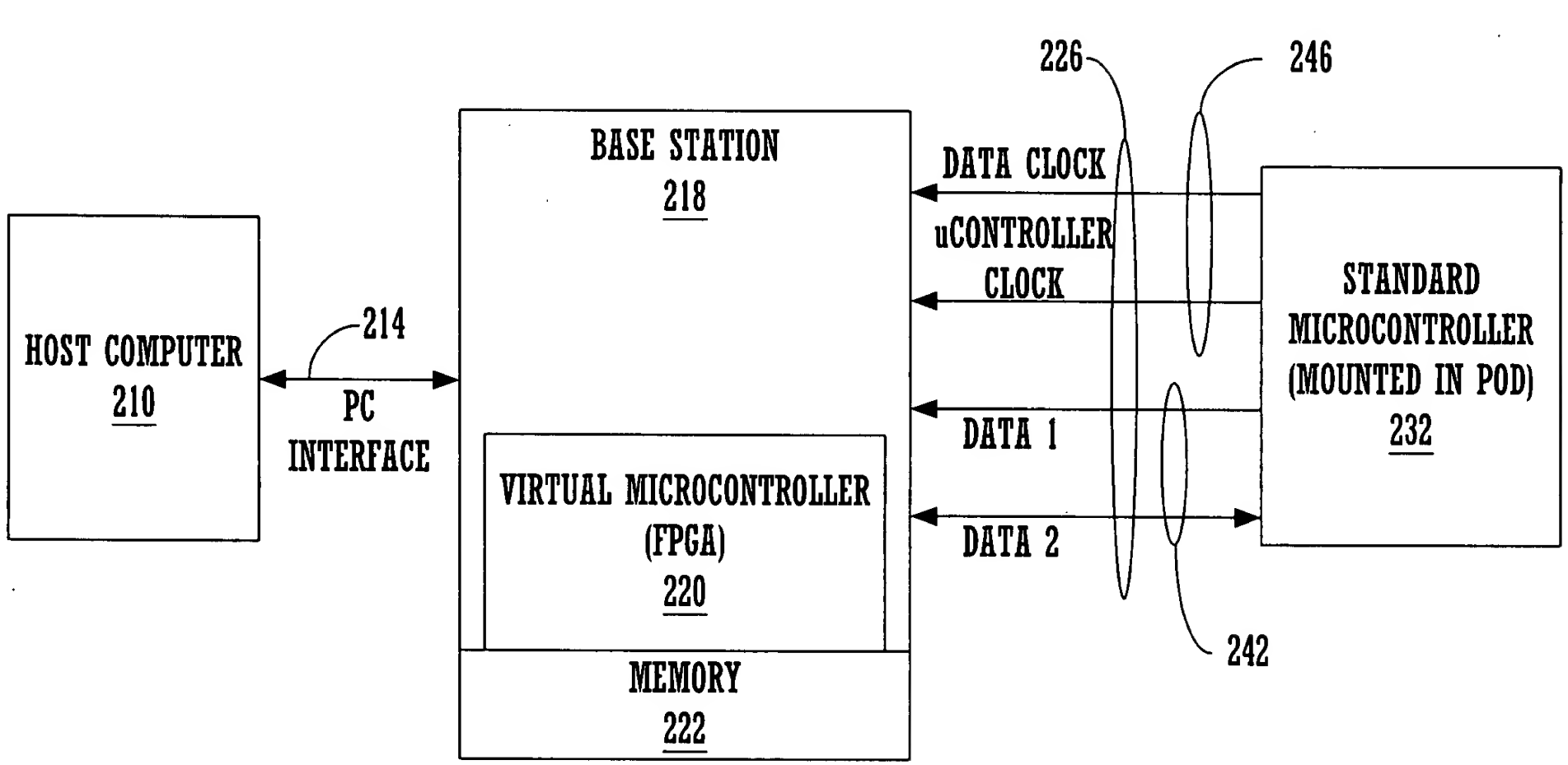
200
226
246
BASE STATION
218
DATA CLOCK
uCONTROLLER
CLOCK
STANDARD
MICROCONTROLLER
(MOUNTED IN POD)
232
HOST COMPUTER
210
214
PC
INTERFACE
DATA 1
VIRTUAL MICROCONTROLLER
(FPGA)
220
DATA 2
242
MEMORY
222

FIGURE 2

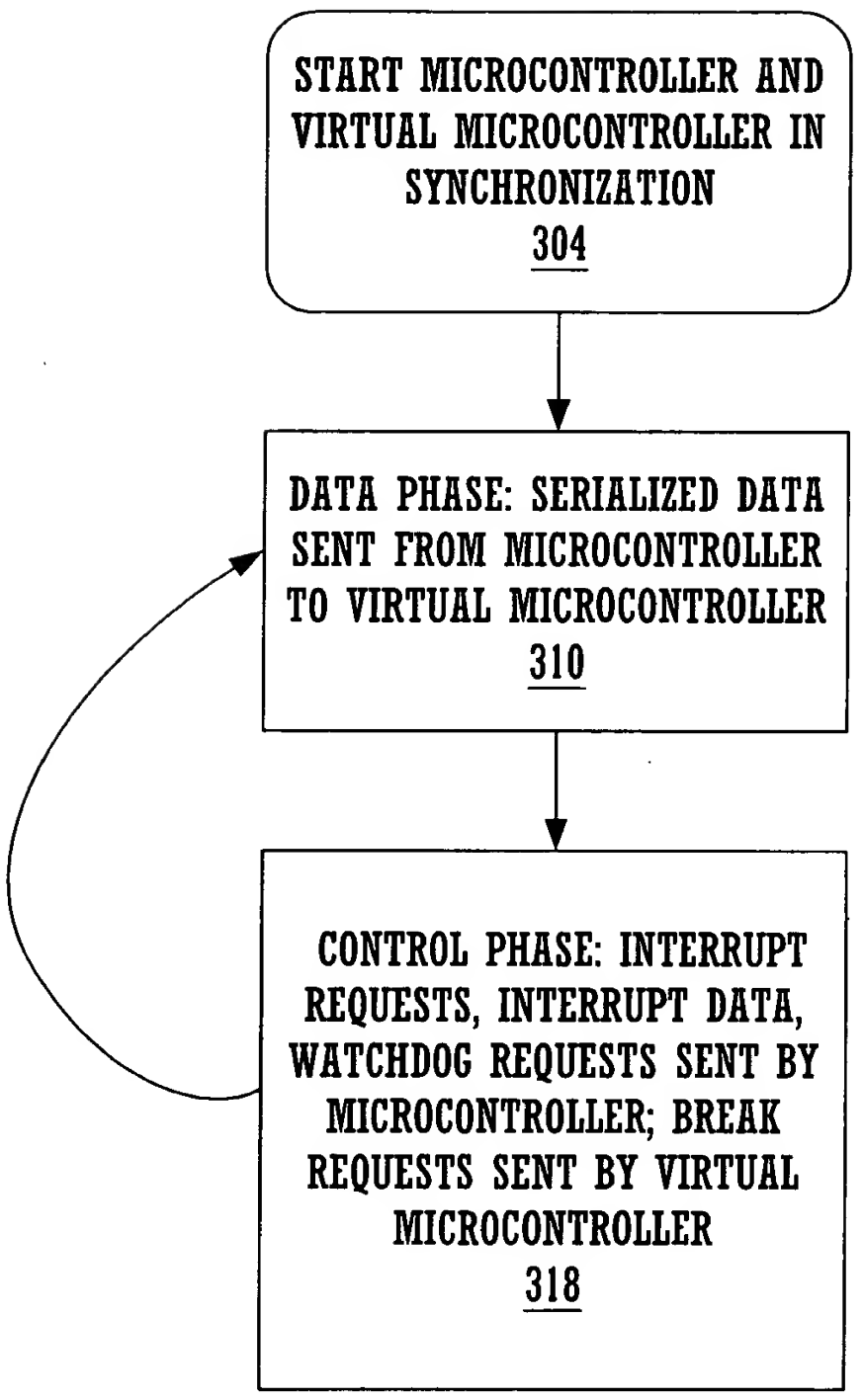
START MICROCONTROLLER AND VIRTUAL MICROCONTROLLER IN SYNCHRONIZATION
304
DATA PHASE: SERIALIZED DATA SENT FROM MICROCONTROLLER TO VIRTUAL MICROCONTROLLER
310
CONTROL PHASE: INTERRUPT REQUESTS, INTERRUPT DATA, WATCHDOG REQUESTS SENT BY MICROCONTROLLER; BREAK REQUESTS SENT BY VIRTUAL MICROCONTROLLER
318

FIGURE 3

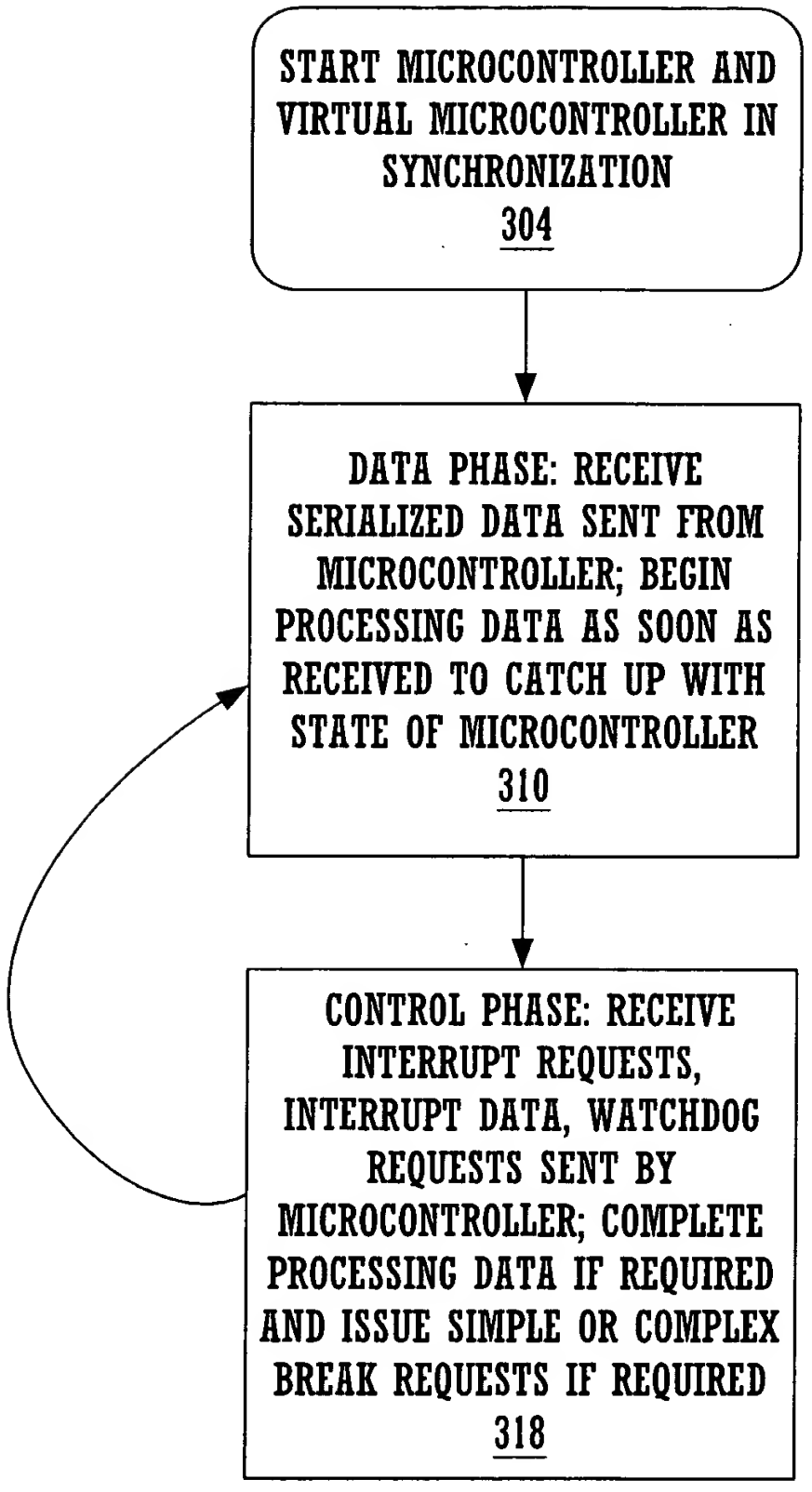
START MICROCONTROLLER AND VIRTUAL MICROCONTROLLER IN SYNCHRONIZATION
304
DATA PHASE: RECEIVE SERIALIZED DATA SENT FROM MICROCONTROLLER; BEGIN PROCESSING DATA AS SOON AS RECEIVED TO CATCH UP WITH STATE OF MICROCONTROLLER
310
CONTROL PHASE: RECEIVE INTERRUPT REQUESTS, INTERRUPT DATA, WATCHDOG REQUESTS SENT BY MICROCONTROLLER; COMPLETE PROCESSING DATA IF REQUIRED AND ISSUE SIMPLE OR COMPLEX BREAK REQUESTS IF REQUIRED
318

FIGURE 4

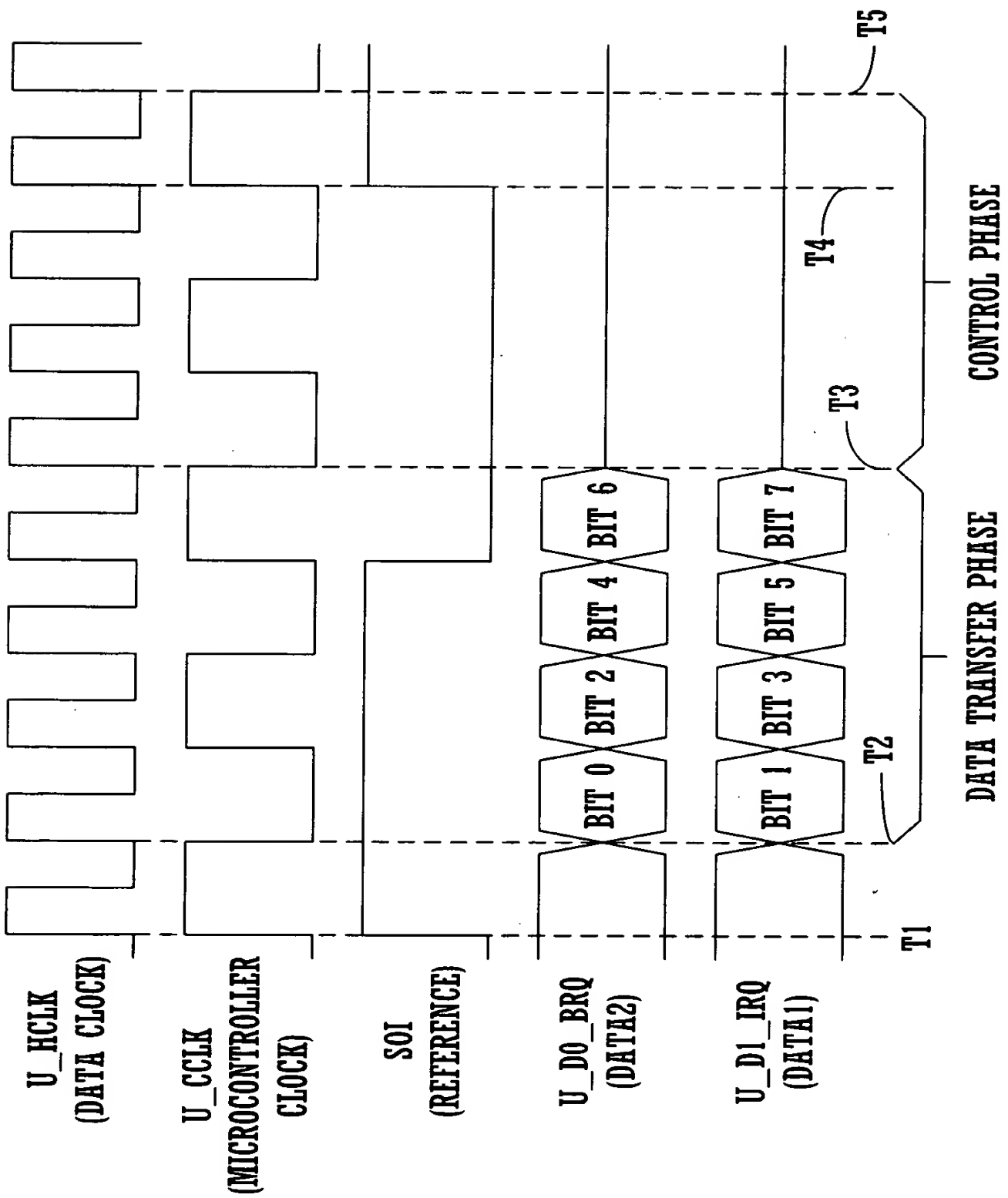
U_HCLK
(DATA CLOCK)
U_CCLK
(MICROCONTROLLER
CLOCK)
SOI
(REFERENCE)
U_D0_BRQ
(DATA2)
U_D1_IRQ
(DATA1)
BIT 0
BIT 2
BIT 4
BIT 6
BIT 1
BIT 3
BIT 5
BIT 7
T1
T2
T3
T4
T5
DATA TRANSFER PHASE
CONTROL PHASE

FIGURE 5